

3.2.1 Number of research papers published per teacher in the Journals notified on UGC website during the year

S.NO	Title of paper	Name of the author/s	Department of the teacher	Name of journal	Year of publication	ISSN number	Link to the recognition in UGC enlistment of the Journal
2023-24							
1	Design and Implementation of 5G LDPC Decoder Architecture with Parallel and Adaptable on FPGA Target	Mr. M. Ramana Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A1.pdf
2	Design and Implementation of 5G LDPC Decoder Architecture with Parallel and Adaptable on FPGA Target	Mr. B. Ajantha Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A1.pdf
3	A Capacitorless Analog Ldo For Output Adjusting The Frequency Of A Four-Stage Amplifier	Mr.A.Prasad	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A2.pdf
4	A Capacitorless Analog Ldo For Output Adjusting The Frequency Of A Four-Stage Amplifier	Mr.K.Ch.Malla Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A2.pdf
5	Design and Implementation of Reed-Solomon Erasure Code (RS EC) Decoders with FPGA Implementation that Detects and Locates Faults in User Memory	Dr.A.Ranganayakulu	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A3.pdf
6	Design and Implementation of Reed-Solomon Erasure Code (RS EC) Decoders with FPGA Implementation that Detects and Locates Faults in User Memory	Mr.D.Satyanarayana	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A3.pdf
7	A Partial Product Reduction Process Integrating Additions and Accumulations to Create a High-Performance Multiply-Accumulate Unit(MAC)	Mr.N.B.Jilani	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A4.pdf
8	A Partial Product Reduction Process Integrating Additions and Accumulations to Create a High-Performance Multiply-Accumulate Unit(MAC)	Mrs.M.Haritha	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A4.pdf
9	Design and Implementation of Multipath Fully Differential OTA Implementation in LT-Spice CMOS Process.	Mrs.N.Swarupa Rani	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A5.pdf
10	Design and Implementation of Multipath Fully Differential OTA Implementation in LT-Spice CMOS Process.	Dr.P.Prasanna Murali Krishna	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A5.pdf
11	DESIGN AND IMPLEMENTATION OF PHASE INTERPOLATION IN ANALYTICAL MODELING OF JITTER IN BANG-BANG CDR CIRCUITS	Mr.K.Ch.Malla Reddy	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A6.pdf
12	DESIGN AND IMPLEMENTATION OF PHASE INTERPOLATION IN ANALYTICAL MODELING OF JITTER IN BANG-BANG CDR CIRCUITS	Mr.A.Prasad	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A6.pdf
13	Design and implementation of an Economical Approach to Test Screening on LT-spice Embedded SRAMs for Low-Power MCUs	Dr.A.Ranganayakulu	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A7.pdf
14	Design and implementation of an Economical Approach to Test Screening on LT-spice Embedded SRAMs for Low-Power MCUs	Mr.D.Satyanarayana	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A7.pdf
15	Design and implementation of a Microcontroller Arithmetic and Logical Unit with Optimized Area, Power, and Performance on FPGA	Mrs.M.Haritha	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A8.pdf

16	Design and implementation of a Microcontroller Arithmetic and Logical Unit with Optimized Area, Power, and Performance on FPGA	Mr.N.B.Jilani	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/A8.pdf
17	High-Efficiency Multicontext MQ Arithmetic Coder Designed using VLSI design on FPGA	Mr. M. Ramana Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A9.pdf
18	High-Efficiency Multicontext MQ Arithmetic Coder Designed using VLSI design on FPGA	Mr. B. Ajantha Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A9.pdf
19	Design and Implementation of Compressors and Quick Binary Counters Produced by Sorting Network on FPGA	Mrs.N.Swarupa Rani(Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A10.pdf
20	Design and Implementation of Compressors and Quick Binary Counters Produced by Sorting Network on FPGA	Dr.P.Prasanna Murali Krishna	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A10.pdf
21	R and Shift: A Fault-Tolerant and Energy-Efficient Approach in Secure Nonvolatile Main Memory on FPGA	Mr. M. Ramana Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A11.pdf
22	R and Shift: A Fault-Tolerant and Energy-Efficient Approach in Secure Nonvolatile Main Memory on FPGA	Mr. B. Ajantha Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A11.pdf
23	Functional Constraints in the Selection of Gate-Exhaustive Two Cycle Faults for Test Generation using LFSR Automatic test pattern generator (ATPG)	Dr.A.Ranganayakulu	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A12.pdf
24	Functional Constraints in the Selection of Gate-Exhaustive Two Cycle Faults for Test Generation using LFSR Automatic test pattern generator (ATPG)	Mr.D.Satyanarayana	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A12.pdf
25	Design and Implementation of approximate High-Order Compressors with Low Power and High Accuracy Approximate Multiplier on FPGA	Mrs.N.Swarupa Rani	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A13.pdf
26	Design and Implementation of approximate High-Order Compressors with Low Power and High Accuracy Approximate Multiplier on FPGA	Dr.P.Prasanna Murali Krishna	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/A13.pdf
27	Design and Implementation of Mechanisms for Faster Updates in FPGA-based Ternary Content-addressable Memory	Dr.A.Ranganayakulu	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B1.pdf
28	Design and Implementation of Mechanisms for Faster Updates in FPGA-based Ternary Content-addressable Memory	Mr.D.Satyanarayana	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B1.pdf
29	Lightening Asynchronous Pipeline Controller with Reusable Delay Path Synthesis on FPGA and LT-Spice	Dr.A.Ranganayakulu	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B2.pdf
30	Lightening Asynchronous Pipeline Controller with Reusable Delay Path Synthesis on FPGA and LT-Spice	Mr.D.Satyanarayana	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B2.pdf
31	Implementation of Effective Modular Adder Designs Using One-Hot Coding and Thermometer on FPGA	Dr.A.Ranganayakulu	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B3.pdf
32	Implementation of Effective Modular Adder Designs Using One-Hot Coding and Thermometer on FPGA	Mr.D.Satyanarayana	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B3.pdf

33	Design and Implementation of Radix-8 Booth Multipliers for High Performance FPGA-Based Accelerators: An Estimate (AxBMs) on FPGA	Mr. M. Ramana Reddy	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B4.pdf
34	Design and Implementation of Radix-8 Booth Multipliers for High Performance FPGA-Based Accelerators: An Estimate (AxBMs) on FPGA	Mr. B. Ajantha Reddy	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B4.pdf
35	Design and Implementation of LPC: An Error Correction Code to Reduce Errors in Three Dimensional(3D) Memories on FPGA	Mrs.M.Haritha	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B5.pdf
36	Design and Implementation of LPC: An Error Correction Code to Reduce Errors in Three Dimensional(3D) Memories on FPGA	Mr.N.B.Jilani	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B5.pdf
37	Design and Analysis of Approximate Booth Multipliers with Low Power and Area Consumption on FPGA	Mrs.M.Haritha	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B6.pdf
38	Design and Analysis of Approximate Booth Multipliers with Low Power and Area Consumption on FPGA	Mr.N.B.Jilani	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B6.pdf
39	Design and Implementation of Programmable Delays in Oscillator-Rings for FPGA-Based True Random Number Generation on FPGA	Dr.A.Ranganayakulu	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B7.pdf
40	Design and Implementation of Programmable Delays in Oscillator-Rings for FPGA-Based True Random Number Generation on FPGA	Mr.D.Satyanarayana	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B7.pdf
41	Design and Implementation of High-Throughput Parallel Hash Join Architecture on FPGA Based SRAM	Mr.K.Ch.Malla Reddy	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B8.pdf
42	Design and Implementation of High-Throughput Parallel Hash Join Architecture on FPGA Based SRAM	Mr.A.Prasad	Electronics and communication engineering	Juni Khyat	2024	2278- 4632	https://www.junikhayatjournal.org/pdf/B8.pdf
43	A Quick And Effective Karatsuba-Based Finite Field Multiplier For FPGA Integration	Mr. M. Ramana Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B9.pdf
44	A Quick And Effective Karatsuba-Based Finite Field Multiplier For FPGA Integration	Mr. B. Ajantha Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B9.pdf
45	Design and Analysis of Digital Signature Accelerators Using Cryptography Based on Ed25519 on FPGA	Mrs.N.Swarupa Rani	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B10.pdf
46	Design and Analysis of Digital Signature Accelerators Using Cryptography Based on Ed25519 on FPGA	Dr.P.Prasanna Murali Krishna	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B10.pdf
47	Implementation of a Novel Approximate (8; 2) Compressor for Applications in Image Processing on FPGA	Mrs.N.Swarupa Rani	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B11.pdf
48	Implementation of a Novel Approximate (8; 2) Compressor for Applications in Image Processing on FPGA	Dr.P.Prasanna Murali Krishna	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B11.pdf
49	Design and Implementation of a Compact True Random Number Generator for Applications Relating to Root of Trust on FPGA	Mr.K.Ch.Malla Reddy	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B12.pdf

50	Design and Implementation of a Compact True Random Number Generator for Applications Relating to Root of Trust on FPGA	Mr.A.Prasad	Electronics and communication engineering	International Journal of Gender, Science and Technology	2024	2040-0748	https://ijgst.com/admin/uploads/B12.pdf
51	A Block Chain Based Distributed Ledger Enhancing Modular Sawtooth Framework for Fact Finding in Digital Forensics	Mrs.T. Deepthi	Computer science and engineering	The International journal of analytical and experimental modal analysis	2024	0886-9367	https://drive.google.com/file/d/1Sq0S3n5PVg2L01hw5Y7sowOILSjvpKCH/view
52	A Learning Based Optimized Hybrid Model for Efficient and Scalable Long Document Classification	Dr. SK Althaf Hussain Basha	Computer science and engineering	Journal of Theoretical and Applied Information Technology	2023	1992 8645	https://www.jatit.org/volumes/Vol101No19/17Vol101No19.pdf
53	Crime Prediction Using Machine Learning Algorithms	Dr. SK Althaf Hussain Basha	Computer science and engineering	International Journal of Computer Science and Mechatronics,	2023	2455-1910	https://drive.google.com/file/d/1c8CvqdPeUg21DPEhlo2Xk9iCXo_9PT5j/view
54	ODC-Net: Bridging Natural Optimization and Deep Learning for Enhanced Outlier Detection in Multidimensional Data	Dr. SK Althaf Hussain Basha	Computer science and engineering	Journal of Xi'an University of Architecture & Technology	2023	1006-7930	https://drive.google.com/file/d/1mFOiPwfOw5VWIC-ITBP3pnwKvuCuS3j/view
55	Paraphrase Extraction by Using Machine Learning Algorithms- A Review	Dr. SK Althaf Hussain Basha	Computer science and engineering	Journal of Basic Science and Engineering	2024	1005-0930	https://yigkx.org.cn/index.php/jbse/article/view/116
56	Data Science and Machine Learning Based Intelligent Model for Student Performance Evaluation System	Dr. SK Althaf Hussain Basha	Computer science and engineering	International Journal of Computer Science and Mechatronics,	2023	2455-1910	